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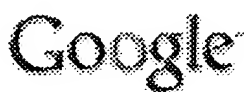
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FPL 2001

Gambit: A Tool for the Simultaneous Placement and Detailed Routing of Gate-Arrays.

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successfully in the context of a compiler that maps applications directly to

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FPGA FPGA. Compiler. Mapper. Estimator. C. VHDL/Verilog. Place. &. Route.

Simulation. ACS Program ... ACS RISC + Reconfigurable Array architectures entering ...

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... it doesn't matter: you write the code, compile it and place in array. ...

For FPGAs that provide the same functionality the place and route time is ...

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matrix. FPGA mapping begins by dividing the circuit into pieces of sequential logic (logic nodes), ... placement and routing in the hand-mapped version. ...

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and execute technology mapping, placement, and routing. Such compilation would be done on a small lean processor coexisting on the FPGA for this purpose, ...

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the previous switch matrix and attempt to route the wire in the ... technology mapping, and place and route. Code Size is the ...

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